Research On Optimisation Methods in Comparator Design

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Abstract: This work presents a discussion of the early latch-type Voltage Sense amplifier, two improved latch comparator designs, and a novel edge-race comparator (ERC). The optimum input DC voltage can be used to increase the yield without changing the structure of the StrongARM and without speed penalty. The improved Miyahara's comparator, with an addition of a charge pump increases the speed by 60%. A bias dynamic comparator with a tail capacitor reduces the average energy consumption to 40% of the previous level. The ERC, consisting of two inverter loops and a distance measurement circuit, is 3.39 times faster at comparing differential voltages of 1mV and 2.73 times less energy efficient than previous work.

1. Introduction

Comparators are important interface circuits in digital-to-analog converters (ADCs), which compare the magnitude of two input voltages to convert an analogue signal into a binary signal. With the development of integrated circuit technology, high speed, low power consumption and high yield comparators are desired. Dynamic comparators fulfil these requirements very well and are the most widely used technique today. But how to further increase the speed and reduce the power consumption is still the current research direction. Three improved dynamic comparators will be investigated later. Besides the dynamic comparators, Minseob Shim et al. proposed a novel comparator based on ring oscillator collapse in 2017, edge-pursuit comparator (EPC), which automatically adjusts power consumption and noise according to the input voltage [1]. The EPC is limited by a very large delay when the differential input voltage is low. The edge-race comparator (ERC) proposed by Haoyang Zhang in 2020 addresses this limitation well, increasing the speed of fine comparing while power consumption is reduced also [2].

This paper is organised as follows. Section 2 briefly describes the development of dynamic comparators and presents three different approaches to improving them. Section 3 investigates the new comparator ERC, and Section 4 gives a comparative analysis of the four comparators studied. A summary is given in Section 5.

2. Research on dynamic comparators

The first dynamic comparator, StrongARM was first presented in 1992 by Toshiba's Kobayashi et al. [3] [4] and B Wicht et al. analyse this latch-type voltage sense amplifier shown in Figure 1 and enhance the yield without speed penalty by changing only one parameter [5]. However, the downside is that it contains numerous stacked transistors that require a high voltage headroom [6] [7].

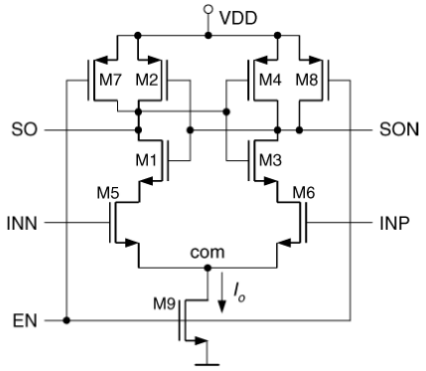


Figure 1. Structure of StrongARM

D. Schinkel et al. proposed a double-tail latch-type comparator in 2007 which solves these issues [7]. It separates the input and latching stages, increasing operating speed and allowing a wider range of common mode input and supply voltage. Miyahara and Elzakker proposed two different variants of two-stage latching comparators in 2008 and 2010 respectively, further improving comparison speed and reducing power consumption [8] [9]. Harijot Singh Bindra et al. add a tail capacitor to further reduce the power consumption of Elzakker's comparator in 2018 and Haoyang Zhang et al. use an extra charge pump to increase the speed of the Miyahara comparator by 60% in 2020 [5] [10].

2.1 Optimization of StrongARM

B Wicht and his team have provided an in-depth theoretical analysis of the StrongARM shown in Figure 1 and have improved the yield without speed penalty of the comparator by selecting the optimum parameters without changing the circuit structure.

The proposed circuit is reset when the EN signal is 0 and when the enable signal goes high, the transient behaviour of the circuit is shown in Figure 2.

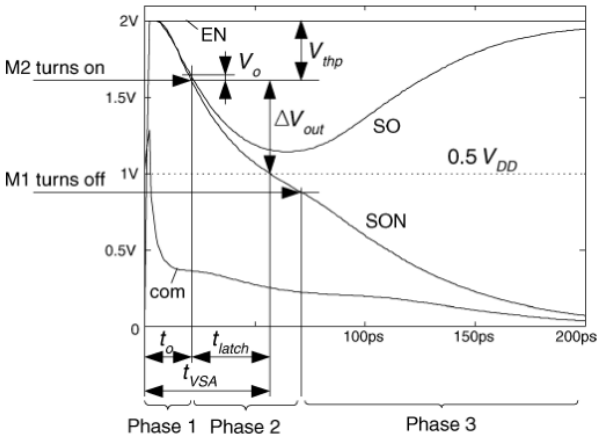


Figure 2. transient behaviour of StrongARM

The delay t_{VSA} shown in Figure 2, which is a sum of t_{wo} and t_{latch}, and the yield Y given in (1) are two main performance parameters to be optimised.

$$Y = \frac{number\ of\ correct\ decisions}{number\ of\ samples} \cdot 100\% \quad (1)$$

Y is the rate of the comparator making the correct decisions, due to random mismatch and systematic offset. To analyse the relationship between random mismatch and the Yield, the subsequent analysis is based on a circuit without systematic offsets, with any imbalance due to random mismatch summarised by the input offset voltage Vos and the imbalance between the output load capacitances represented by ECL. The output capacitance at SO is C_L, while the output capacitance at SON is (1+ECL) *C_L, ideally with an ECL of 0. The input differential signal $V_{IN,}$ the power supply

V_{DD} and the input DC voltage V_{INDC} are the main parameters which determine the yield Y. Based on Monte Carlo simulation with 1000 samples, yield Y can be described as the probability P for V_{OS} is lower than or equal to where V_{OS} follows a Gaussian probability distribution plotted in Figure 3.

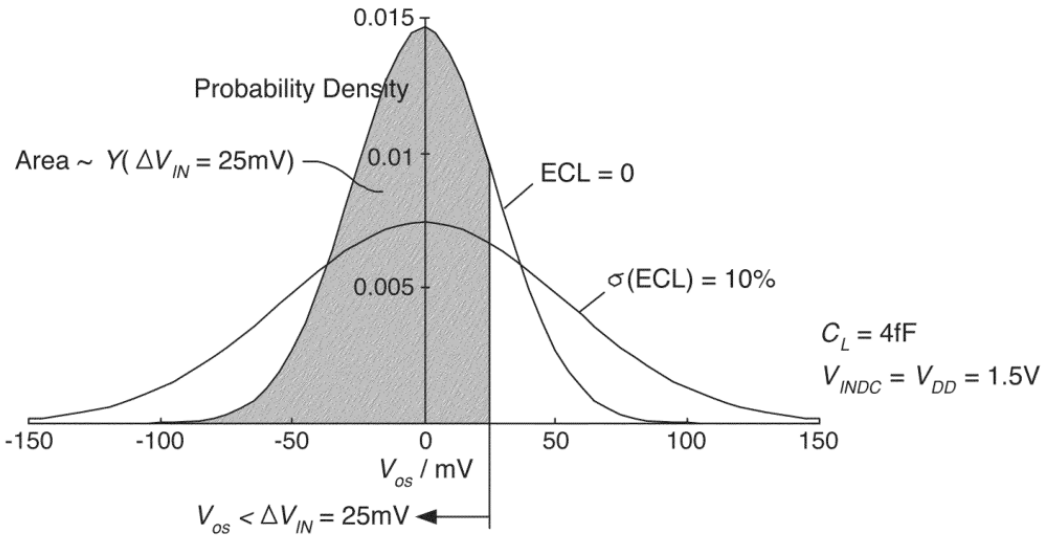


Figure 3. Probability density function of VOS

Yield Y can be described by

$$Y(\Delta V_{IN}) = P(V_{OS} \le \Delta V_{IN}) = \Phi\left(x = \frac{\Delta V_{IN}}{\sigma_{OS}}\right) = \frac{1}{2} + \int_0^x \varphi(y)dy \tag{2}$$

Where $\varphi(y)dy$ is given by

$$\varphi(y) = \frac{1}{\sqrt{2\pi}} e^{-\frac{y^2}{2}} \tag{3}$$

Yield Y is only determined by σ_{OS} which is the standard deviation of V_{IN}, but it is more appropriate to establish the relationship between yield Y and V_{IN} directly, as shown in Figure 4, than to obtain the distribution of V_{OS} and hence yield through Monte Carlo simulation. In addition, Figure 4 shows the effect of different levels of load capacitance on yield.

It is effective to improve yield by reducing the input DC voltage. The relationship between V_{INDC} and the bias current through the transistor M9 I_O is given by

$$I_O \approx 2\beta(V_{INDC} - V_{th})^2 \left(1 - \frac{0.75}{1 + \frac{V_{DD} - V_{th}}{V_{INDC} - V_{th}}}\right)^2 \tag{4}$$

The lower V_{INDC} results in a higher Io, thus the initial voltage difference Vo between SO and SON is higher. Like V_{OS}, a higher V_o will optimize the yield. Figure 5 shows yield Y versus input differential voltage VIN for different input DC voltages when V_{DD} is 1.5V.

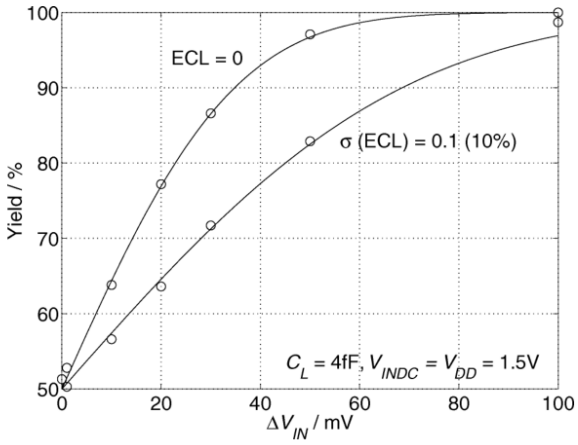


Figure 4. Yield versus input voltage difference ΔV_{IN} under different ECL

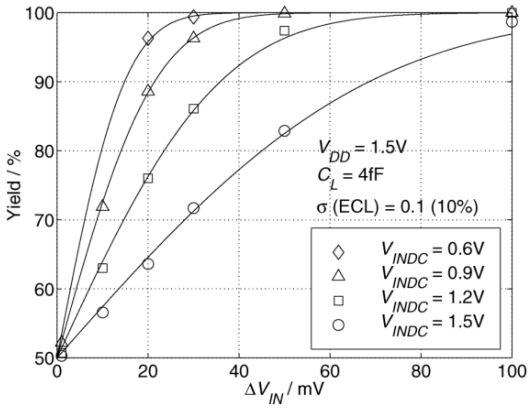


Figure 5. Yield versus input voltage difference for different V_{INDC}

It is necessary to increase the yield without decreasing the speed. When V_{INDC} decreases, the delay in the first phase increases due to the larger bias current I_o, but the larger initial differential voltage V_o accelerates the second phase.

In order to find a balance between speed and yield, the FOM is defined by

$$FOM(V_{INDC}) = \frac{\frac{Y(V_{INDC})}{t_{VSA}}}{\min(t_{VSA})} \tag{5}$$

Which describes the relationship between Yield Y and delay t_{VSA} for different V_{INDC}, and a higher FOM is desired. The curve for the FOM and the graphs of V_{INDC} versus delay and yield are given in Figure 6. It can be observed that when V_{INDC} drops to $0.4V_{DD}$ the yield reaches a maximum but the delay increases. When V_{INDC} does not fall below 0.6vdd, the delay hardly changes. The function pattern of FOM shows that the optimal value of V_{INDC} for different V_{DD} is between $0.6V_{DD}$ and $0.8V_{DD}$. As a rule of thumb, $0.7V_{DD}$ is always appropriate, which is the foremost conclusion of the analysis for StrongARM and is used by most circuits today.

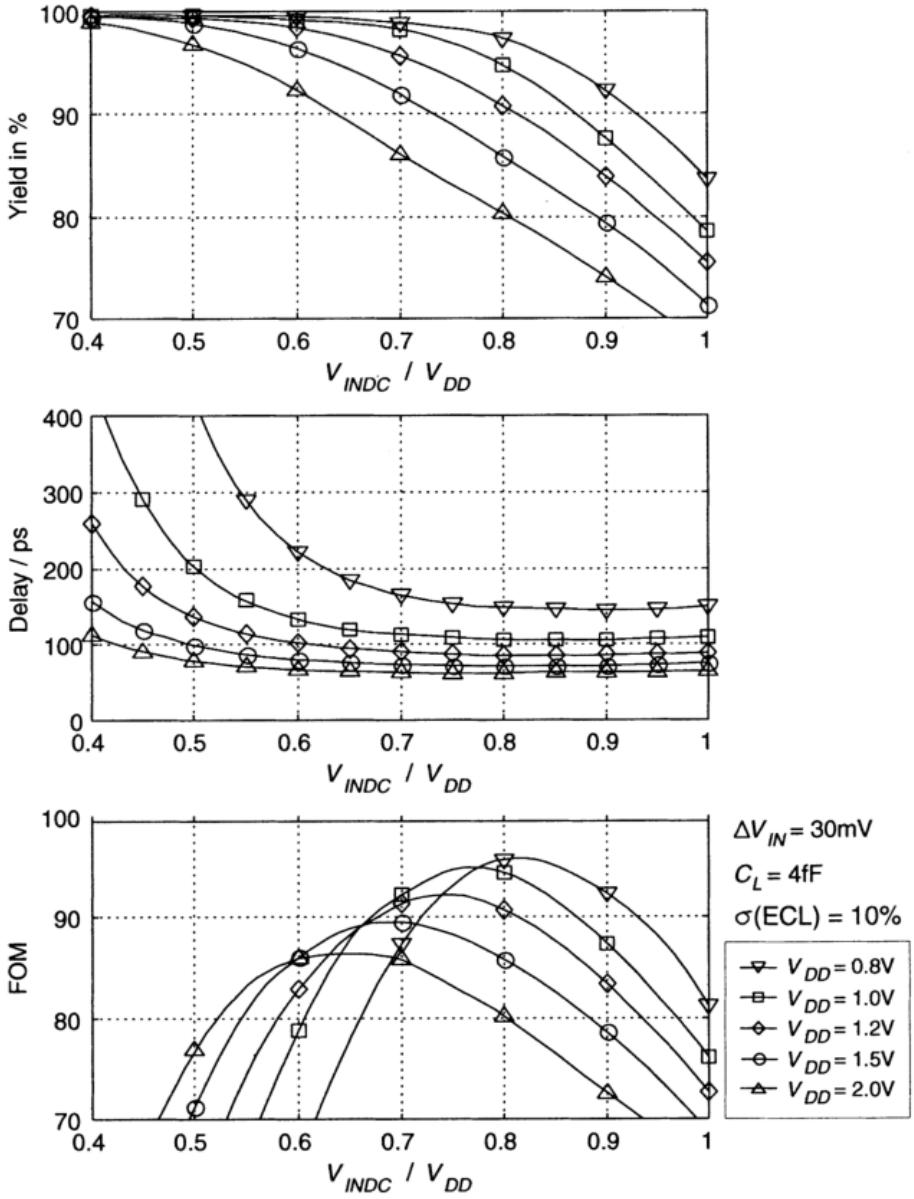


Figure 6. Yield, Delay and FOM versus different V_{INDC}

2.2 Dynamic bias comparator

The proposed comparator is an improvement on the Elzakker's comparator of Figure 7, which is a modified double-tail latch-type comparator that reduces the power consumption. Figure 8 shows the dynamic bias comparator, which uses a tail capacitance and a tail transistor M3a to replace the transistor M3 in Figure 7, while the transistor M3b is used to reset the tail capacitance to ground.

The comparator will be reset when CLK is 0, and when CLK equals to V_{DD}, M3b, M4,5, M12, and M13 turn off. M3a turns on and the node Di+ and Di- of C_P start discharging and result in the common-mode current which generates the tail current I_{TAIL} that charges the tail capacitor

C_{TAIL}. Thus, the increasing V_{CAP} resulting from the C_{TAIL} lowers the differential pair's gate–source voltage, V_{GS}, and so provides a dynamic bias to the differential pair during the comparison phase.

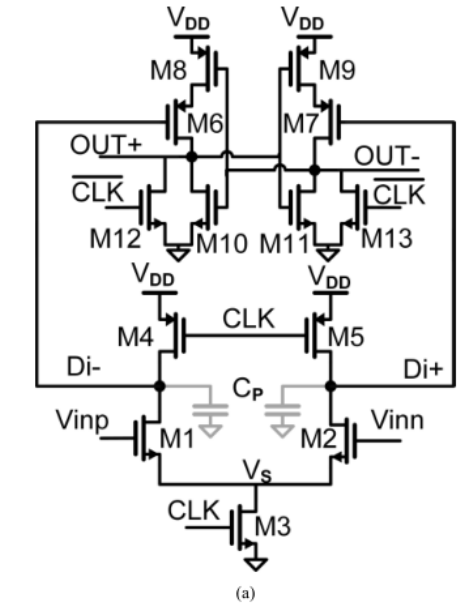


Figure 7. Elzakker's comparator and the simulation of transient behaviour

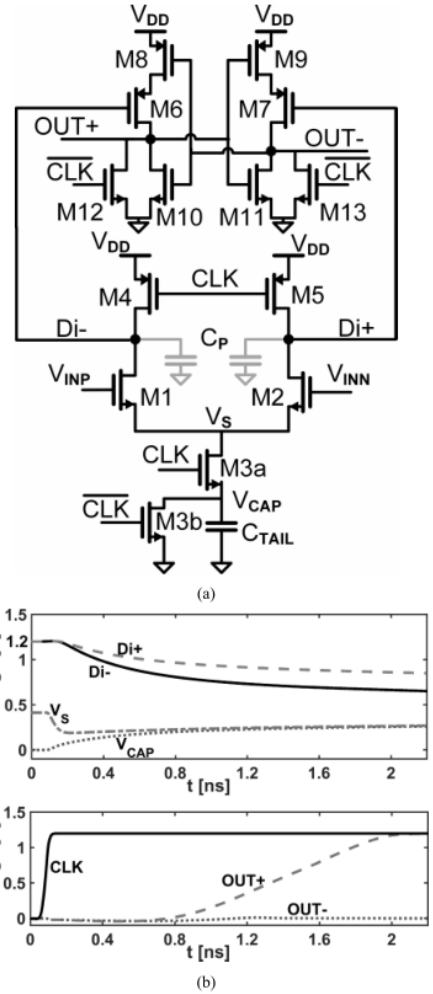


Figure 8. Proposed comparator and the simulation of transient behaviour

The pre-amplifier consumes approximately 80% of the total power consumption, and the energy consumed by the pre-amplifier P_{pre} in the proposed comparator is given by

$$P_{PRE} = 2 \cdot C_P \cdot V_{DD} - C_P \cdot V_{DD} \cdot (V_{D1} + V_{D2}) \tag{6}$$

while V_{D1} and V_{D2} are the voltages of node Di+ and Di-.

The conventional pre charge energy is

$$P_{CON} = 2 \cdot C_P \cdot {V_{DD}}^2 \tag{7}$$

which is less than the proposed one.

The mathematic analysis of the voltage gain of dynamic bias pre-amplifier is shown as

$$A_V(T_{INT}) = \frac{C_{TAIL}}{2n \cdot C_p} \frac{V_S(T_{INT})}{\frac{kT}{q}} \tag{8}$$

$$V_S(T_{INT}) = \frac{2\Delta V_{Di,CM}(T_{INT}) \cdot C_p}{C_{TAIL}} \tag{9}$$

$$\Delta V_S(T_{INT}) = \frac{C_{TAIL}}{C_{TAIL} + 2C_p} V_{DD} \tag{10}$$

The Di node will not be totally discharged to the ground, even under the extremely non-ideal operating circumstances. As a result, the proposed comparator consumes less power than Elzakker's comparator.

To compare the performance, both Elzakker's comparator and the dynamic bias comparator are fabricated on the standard 65-nm CMOS process. The consumption versus input differential voltage for different V_{CM}. For 1mV differential input at V_{CM}=0.6 V, the dynamic bias consumes 34f per comparison while Elzakker's comparator's consumption is 88fJ/comparison. The output common voltage drops at the Di nodes ($\Delta D_{Di,CM}$) is increased because of the increasing V_{CM}. Therefore, a higher V_{CM} leads to higher power consumption which is verified by Figure 9.

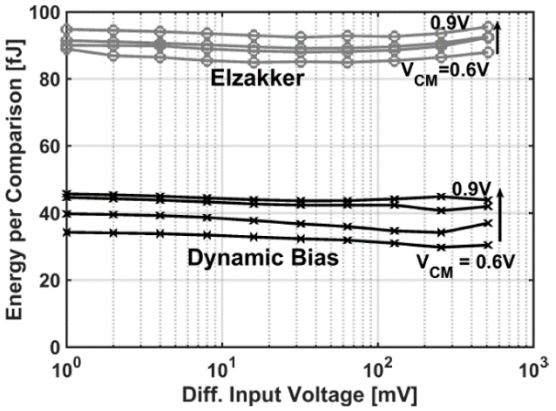


Figure 9. Measure power consumption

Noise is another important performance that need to be considered. The gm/I_d and the input referred noise voltage versus the V_{ov} are shown in Figure 10. The gm/I_d of the proposed comparator is higher than Elzakker's comparator and the power consumption of the proposed one is lower, which is measured and shown in Figure 11.

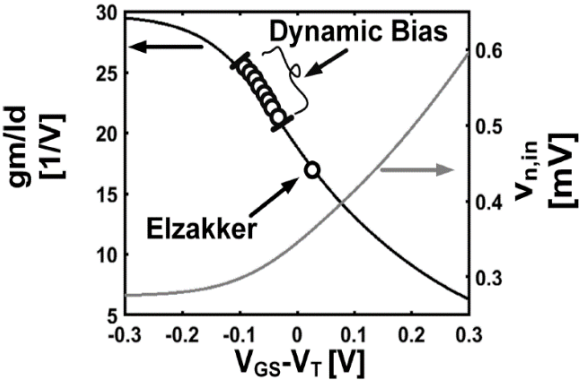


Figure 10. gm/Id and noise voltage (calculated) versus V_{OV}

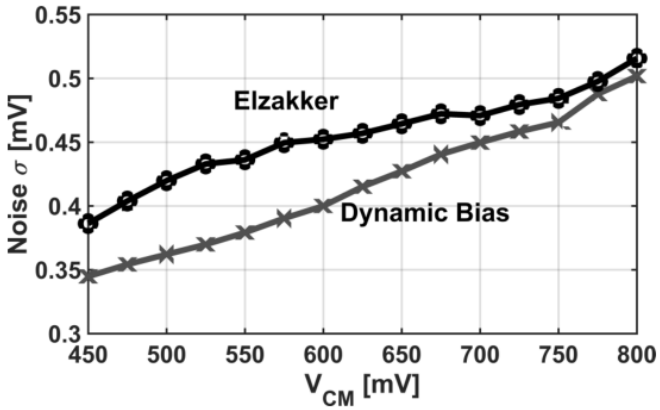


Figure 11. Measured Noise versus V_{CM}

Also, higher V_{CM} causes higher V_{OV}, which results in a lower gm/I_d according to Figure 10. Therefore, the noise increases with the increasing V_{CM}.

2.3 Improved Miyahara's comparator

The proposed comparator given in Figure 12 adds an extra charge pump to the classic Miyahara's comparator shown in Figure 13, which make the comparing speed 60% faster than before while maintain the same noise level.

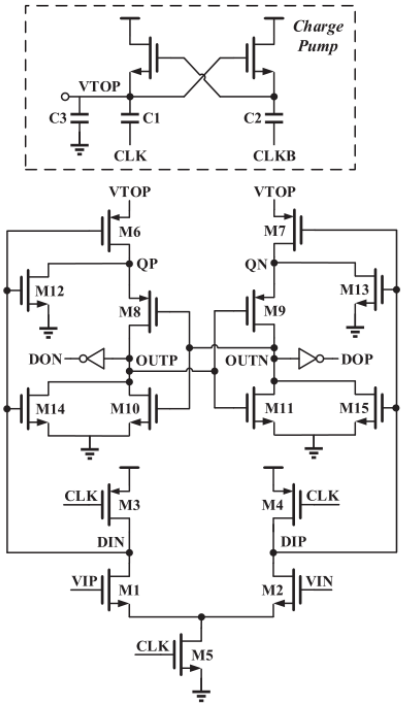


Figure 12. proposed comparator

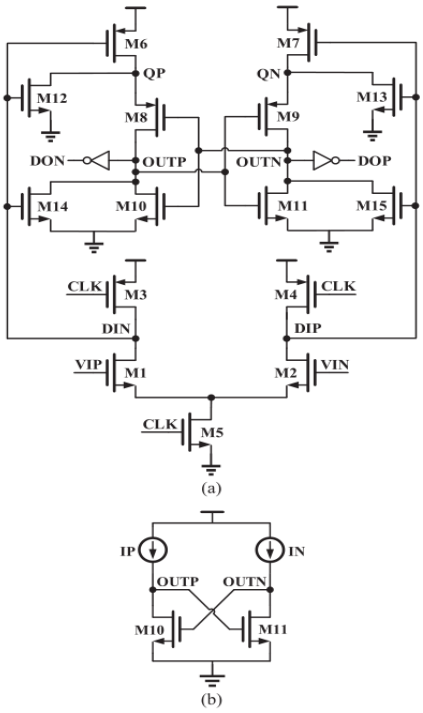


Figure 13. Miyahara's comparator

There are three phases for a Miyahara's comparator, which is the reset phase, the amplification phase, and the regeneration phase. Consider t=0 as the start of the regeneration phase, the differential output voltage is given by

$$V_d(t) = V_{d0} \cdot \mathrm{e}^{t/\tau_u} \tag{11}$$

Where the V_{d0} is the initial output voltage at t=0, and the τ_u is given by

$$\tau_u = \frac{C_{out2}}{g_{m10,11}} \tag{12}$$

Where C_{out2} is the parasitic capacitance at the second-stage amplification phase and g_m is the transconductance of MOSFET. Thus, the higher gm leads to less time in regeneration phase.

The proposed comparator connects the source of M6,7 and the bulk of M9~10 to V_{top} which is generated by a charge pump instead of V_{DD}. V_{top} is equal to VDD when CLK=0, and when CLK goes high, V_{top} rise to $1.16V_{DD}$. Due to this change, when CLK=1, the V_{top} rise, and the second-stage amplification phase starts immediately instead of delaying until DIP and DIN drop to V_{DD}-V_{th} as Miyahara's comparator. As can be seen in Figure 14, the proposed comparator's second-stage amplification is 24ps earlier than the original one and the current is 3 times larger due to higher gate voltage. In addition to the currents shown in Figure 14, the currents of M10, 11 are also increased by a factor of 3. This increases the transconductance and reduces the regeneration time, further increasing the speed of the comparator.

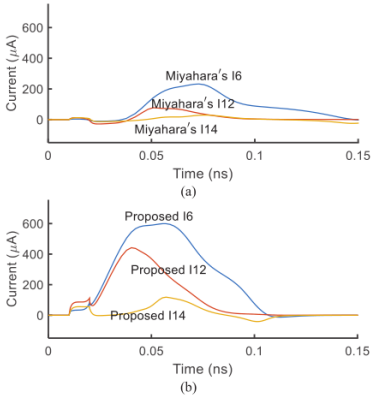


Figure 14. Current through M6, M12, and M14 when CLK=1

From the post-layout simulation results shown in Figure 15, the proposed comparator speed is faster by 56% when comparting a 0.5mV differential input.

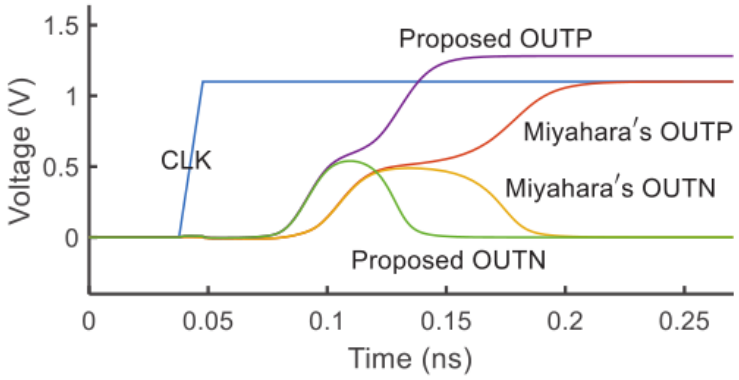


Figure 15. transient behaviour of the proposed comparator and the Miyahara's comparator

Both Miyahara's comparator and the proposed one are manufactured in 40nm CMOS process. The size of the Miyahara's comparator is $63\mu m^2$, the proposed comparator is slightly larger at $182\mu m^2$, due to the use of additional capacitors.

It can be seen from Figure 16 that the speed of the proposed comparator is 60% faster when V_{diff}=1mV. The input-referred noise of the proposed one is $430\mu V$ and $580\ \mu V$ is for Miyahara's. The power consumption of the proposed comparator is 47% larger than that of Miyahara's comparator at V_{diff}=1V, F_{clk}=1GHz due to a higher working voltage.

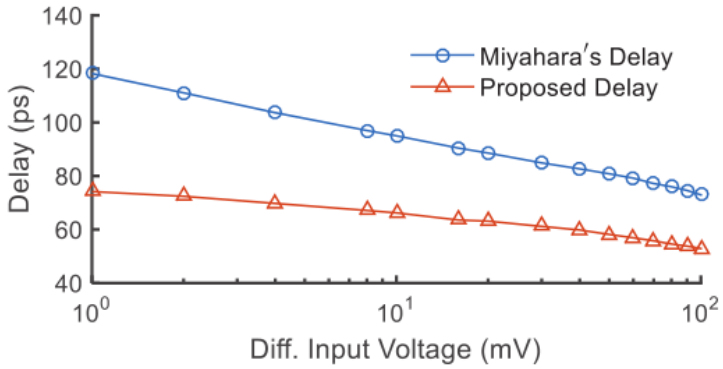


Figure 16. Measured Delay versus Differential input voltage

3. Edge-Race Comparator

To overcome the large delay of the EPC, the edge-race comparator (ERC) is proposed. Similar to the EPC, ERC can adapt its power consumption, delay and noise automatically based on the input voltage, which is ideal for low-power high-resolution SAR ADCs. The difference is the ERC separates one loop into two, resulting in 3.39 times faster and 2.73 times lower power consumption than the EPC when comparing 1-mv inputs.

Figure 17 shows the proposed comparator. In common with the EPC, it also consists of two fly-by-night gates and an inverter delay unit, which is controlled by the differential inputs Vip and Vin, with the difference that the single loop is converted into a double loop. When START=1, the edges generated in the two loops compete until the distance between them exceeds the pre-set value d0, which is 2 invert delays, and a comparison result is generated. The advantage of the ERC is the faster comparison, since 2 inverter delays is a suitable d0 value in ERC, whereas the d0 value of the EPC depends on the number of inverters in the loop, which in Figure 18 is 5 inverter delays.

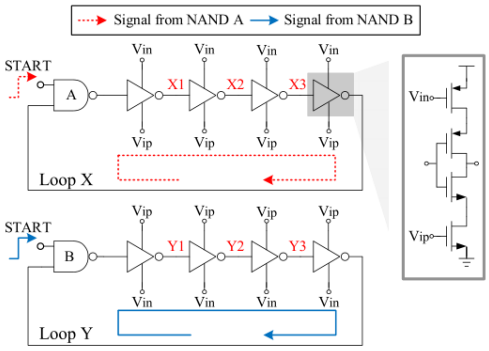


Figure 17. circuit structure of ERC

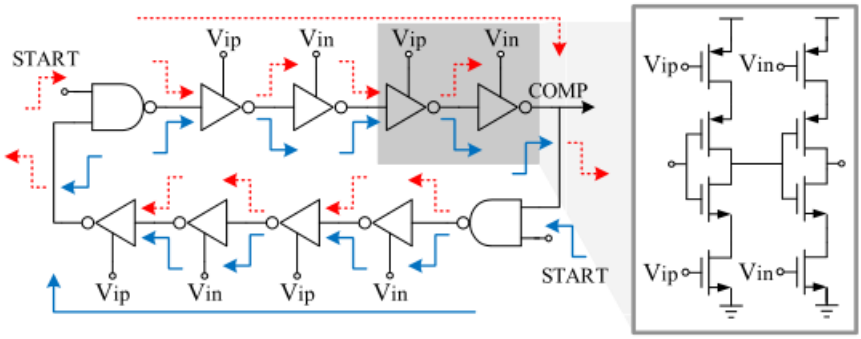


Figure 18. Circuit structure of EPC

In addition to d0, the comparison time of the EPC and ERC is also related to the magnitude of the input differential voltage and the comparison time can be given by

$$t_{Comp} \approx \frac{C_L V_{dd} d0}{g_m(V_{ip}-V_{in})} \tag{13}$$

where C_L is the load capacitance of each delay unit and g_m is the transconductance of the transistor connecting Vip and Vin.

The power consumption of the ERC mainly comes from the two loops and the inverter in the measurement circuit and is proportional to the comparison time. It follows from (13) that the comparison time is inversely proportional to the input voltage range, so the ERC is quite energy efficient in coarse comparisons and only consumes more energy in fine comparisons.

To analyse the noise, each loop can be thought of as a voltage-controlled inverter chain, with noise causing random variations in the propagating edge. The input-referred root mean square (rms) noise σ_n is given as (14) when both Vip and Vin are approximately $V_{DD}/2$.

$$\sigma_n = \frac{1}{\sqrt{N \cdot C_L}} \cdot \frac{2I_{SS}\sqrt{\alpha kT}}{V_{DD} g_m} \tag{14}$$

where N is the number of inverter delay units, I_{SS} is the current flowing through the inverter delay units, αk is a constant and T is the absolute temperature. Noise is negatively correlated with comparison time, and in fine comparisons, noise is lower due to longer comparison times and larger N.

Figure 19 shows the simulation results for the number of delay units versus the comparison time in pre-layout simulation. The number of inverters drawn in figures 18 and 19 is only an example, in practice the number of inverters required varies depending on the magnitude of the input voltage. As can be seen from the simulation results, the value of d0 for the ERC is a pre-set constant, while d0 for the EPC grows linearly with the number of inverters and the comparison time.

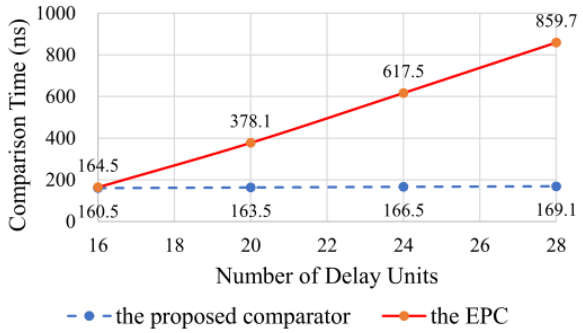
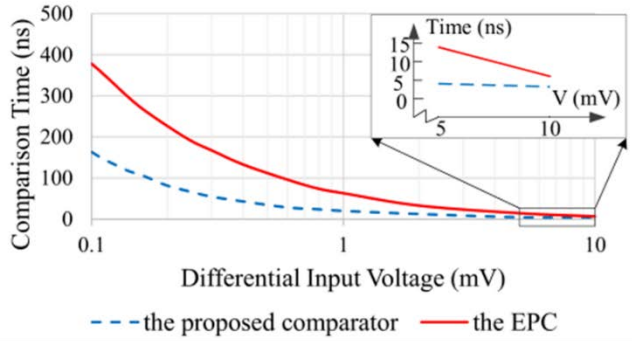
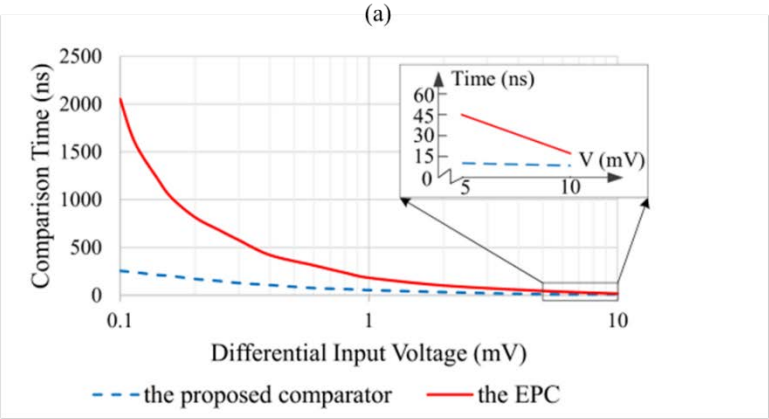


Figure 19. Number of delay units versus comparison time at Vip−Vin=0.1mV.

Figure 20 shows the comparison time versus differential input voltage under pre-layout and post-layout. Comparing the difference in Figure 20, it can be seen that the ERC is better able to resist the interference of the capacitors in the post-layout due to longer distance of two loops in layout.



(a)



(b)

Figure 20. comparison time versus differential input voltage under (a) pre-layout and (b) post-layout

Comparing the power consumption in the postsim with the measurement shown in Figure 21, the measured value is smaller than the simulation result of post-layout value due to the variation in the tape out process, while the power consumption of the ERC is smaller than the EPC due to the reduction in the comparison time.

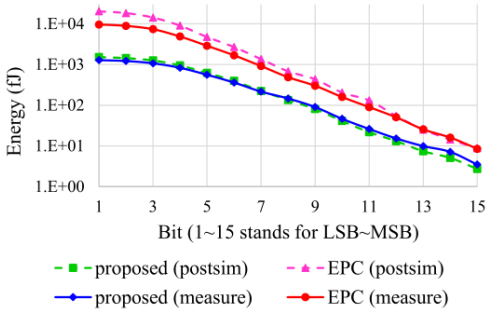


Figure 21. Average energy per comparison versus SAR ADC bit position

4. Discussion

Table 1. Comparison of four comparators

	StrongARM	Dynamic bias comparator	Improved Miyahara's comparator	Edge-Race comparator
Technology	130nm	40nm	40nm	40nm
V_{DD}	-	1.2V	1.1V	-
Power consumption (fJ/comparison at 1mV)	-	34fJ	47% larger	1500fJ
Delay	-	-	80ps	54ns
Noise		0.35mV	0.58mV	0.074mV (20-unit delays)

Table 1 summarises the performance of the four comparators. The three latching comparators optimise yield, delay, and power consumption, but none can optimise both power and delay. B Wicht and his team selected appropriate parameters to improve the performance of the circuit, unlike the other two latching comparators which optimise by changing the structure of the previous circuit.

The ERC is a novel comparator that solves the problem of the long delay time of the EPC but is still not as fast as the latch comparator. Its power consumption is much greater than the three latch-type comparators, and its chip area is larger due to the presence of measurement circuits. These are all further optimisations that need to be made.

5. Conclusion

The designs presented in this paper are dedicated to the implementation of high-speed, low-power comparators. To increase the yield of the StrongARM without speed compensation, the FOM was introduced to confirm that 0.6VDD to 0.8VDD is the optimal range for the input DC voltage. In such a case, the delay of the StrongARM is mainly determined by the size of the transistor. The dynamic bias comparator which adds a tail capacitor to the Elzakker's design reduces the power consumption significantly. Also, a charge pump is added to the Miyahara's improves the speed by 60%. The ERC which is totally different with convention comparators can adjust the noise and power automatically while comparing differential voltages of 1mV, the post-layout simulation results of delay is only 54.2ns, which is an optimal value.

References

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